

Case Study: Verification of Translation Lookaside Buffer

Using UniTESK Technology and CTESK Tool



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Overview

The UniTESK technology and CTESK tool were applied to a Verilog model of translation lookaside buffer (TLB) of MIPS64-compatible microprocessor. TLB is a buffer that is used to translate virtual addresses into physical ones.

The memory of the TLB under test comprises three buffers: a 4-entries instruction micro TLB (ITLB), a 4-entries data micro TLB (DTLB), and a large 64-entries joint TLB (JTLB). The purpose of the micro TLBs is to allow two address translations to be performed simultaneously — one for an instruction fetch address (via the ITLB) and one for a data load/store address (via the DTLB).

Besides the address translation operations, TLB implements operations for reading entry from the buffer, writing entry to the buffer, and probing if the entry exists in the buffer.

Specification and Test Development

Part of the requirements on the TLB under test was formulated by the developers, while the others were derived from the technical documentation. A total number of the requirements is about a hundred. TLB requirements partitioning is shown in the table below.

Operation	Number of requirements
Read	7
Write	9
Probe	8
Data Address Translation	38
Instruction Address Translation	37
Total	99

Requirements on each operation were represented in the form of preconditions and postconditions of microoperations. It should be emphasized that all requirements were cheaply formalized. The volume of specifications is about 2.5 KLOC in SeC language (specification extension of C).

The total labor costs of the testbench development are 2.5 man-months.

Detected Bugs

We have found 9 errors in the TLB implementation including critical ones.

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