Case Study: Verification of Arithmetic Coprocessors

Using MicroTESK Technology

http://www.unitesk.com

Institute for System Programming
Russian Academy of Sciences
25, B. Kommunisticheskaya,
Moscow, 109004, Russia

Phone: +7 (495) 912 5317
Fax: +7 (495) 912 1524
E-mail: info@unitesk.com
http://www.ispras.ru

Institute for System Programming of RAS

Overview

MicroTESK technology was applied to verification of floating-point arithmetic coprocessors (CP1 and CP2).

The CP1 coprocessor implements 114 instructions. All instructions can be clustered into 5 groups:

- floating-point arithmetic (38 instructions)
- branches (6)
- type conversion (33)
- memory (19)
- move (18)

The CP2 coprocessor implements 75 instructions. All instructions can be clustered into 6 groups:

- complex arithmetic (33 instructions)
- branches (4)
- comparison (16)
- memory (12)
- move (8)
- control operations (2)

Specification and Test Development

We used quadruples of instructions as test cases. Test situations were directed to the dependency resolution mechanisms of the coprocessors.

The tables below show volume of test descriptions in lines of code without comments (LOCWC).

Table 1: CP1 generator description

Type of description	Volume, LOCWC	Volume, Percentage
Specification of subsystems	1650	25.5%
Specification of instructions	3000	46.5%
Test situations	1800	28.0%
Total	**6450**	**100.0%**

Table 2: CP2 generator description

Type of description	Volume, LOCWC	Volume, Percentage
Specification of subsystems	2350	20.5%
Specification of instructions	5600	48.5%
Test situations	3600	31.0%
Total	**11550**	**100.0%**

Detected Bugs

We have found more then 10 errors in the RTL models of the coprocessors and more than 10 errors in the coprocessors' simulators (reference models).