

Case Study: Verification of L2 Cache

Using UniTESK Technology and CTESK Tool



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Overview

The UniTESK technology and CTESK tool were applied to Verilog model of L2 cache of MIPS64-compatible microprocessor. The L2 cache under verification is a direct-mapped 256 KB cache that consists of 8192 rows. Each row contains data (four 64-bit double words), tag (18 upper bits of physical address), and control bits (V – Valid and W – Writeback).

The L2 cache serves both data and instructions. It implements operations for loading and storing data, loading instructions, modifying control bits and tags in cache rows. It also supports special snoop reading, writing, and writeline operations. Some of operations can be started in parallel way with a maximum parallelism level of three. E.g. it is possible to start a loading of instruction with a loading of data and with any snoop operation in parallel.

Specification and Test Development

Part of the requirements on the L2 cache under test was formulated by the developers, while the others were derived from the technical documentation. A total number of the requirements is more than one hundred. L2 cache requirements partitioning is shown in the table below.

Operation	Number of requirements
Load Data	21
Store Data	6
Load Instruction	35
Cache	33
Snoop Read	9
Snoop Write	11
Snoop Writeline	5
Total	120

Requirements on each operation were represented in the form of preconditions and postconditions of microoperations. It should be emphasized that all requirements were cheaply formalized. The volume of specifications is about 3 KLOC in SeC language (specification extension of C).

The total labor costs of the testbench development are 6 man-months.

Detected Bugs

We have found 12 errors in the L2 cache implementation including critical ones.

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